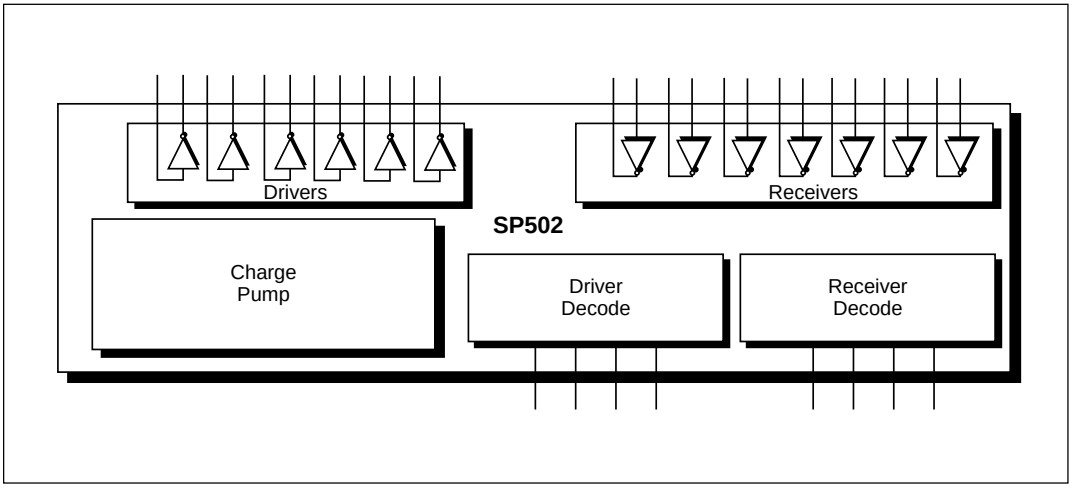
SP502

Multi–Mode Serial Transceiver

- Single-Chip Serial Transceiver Supports Industry-Standard
- Software-Selectable Protocols:
  - — RS-232 (V.28)
  - — RS-422A (V.11, X.27)
  - — RS-449
  - — RS-485
  - — V.35
  - — EIA-530
- Programmable Selection of Interface
- +5V-Only Operation
- Six (6) Drivers and Seven (7) Receivers
- Surface Mount Packaging

DESCRIPTION…

The **SP502** is a highly integrated serial transceiver that allows software control of its interface modes. It offers hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, and EIA-530. The **SP502** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation.



SPECIFICATIONS

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= 3.2mA
V_{OH}	2.4			Volts	I_{OUT}= 1.0mA
RS-485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
HIGH Level Output			+6.0	Volts	
LOW level Output			-0.3	Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Balance			±0.2	Volts	
Open Circuit Voltage			±6.0	Volts	
Output Current	28.0			mA	R_L=54Ω
Short Circuit Current			±250	mA	Terminated in -7V to +12V
Transition Time			120	ns	Rise/fall time, 10%-90%
Maximum Transmission Rate	5			Mbps	
RS-485 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+12.0	Volts	(a)-(b)
LOW Threshold	-7.0		-0.2	Volts	(a)-(b)
Common Mode Range	-7.0		+12.0	Volts	
HIGH Input Current					Refer to graph
LOW Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	Over -7V to +12V common mode range
Input Impedance			1	Unit Load	Refer to graph
V.35 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±0.44		±0.66	Volts	With termination network; R_L=100Ω
Output Impedance	50		150	Ω	With termination network
Transition Time			40	ns	
Maximum Transmission Rate	5			Mbps	
V.35 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Receiver Sensitivity			±0.2	Volts	Over -7V to +12V common mode range
Input Impedance	90		110	Ω	With termination network

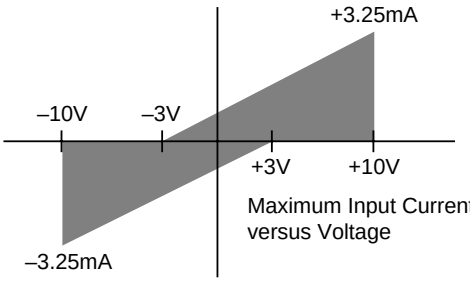
SPECIFICATIONS (Continued)

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Differential Output	±2.0		±5.0	Volts	R_L=100Ω
Open Circuit Voltage,V_O			±6.0	Volts	
Balance			±0.4	Volts	$\|V_T\| - \|\overline{V_T}\|$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			60	ns	Rise/fall time, 10%-90%
Maximum Transmission Rate	5			Mbps	
RS-422 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+6.0	Volts	(a)-(b)
LOW Threshold	-6.0		-0.2	Volts	(a)-(b)
Common Mode Range	-10.0		+10.0	Volts	
HIGH Input Current					Refer to graph
LOW Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			kΩ	
RS-232 DRIVER					
TTL Input Level					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
HIGH Level Output	+5.0		+15	Volts	R_L=3kΩ, V_{IN}=0.8V
LOW Level Output	-15.0		-5.0	Volts	R_L=3kΩ, V_{IN}=2.0V
Open Circuit Voltage	-15		+15	Volts	
Short Circuit Current			±100	mA	
Power Off Impedance	300			Ω	
Slew Rate			30	V/µs	R_L=3kΩ, C_L=15pF
Transition Time			1.56	µs	
Maximum Transmission Rate	120			Kbps	
RS-232 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold		1.7	2.4	Volts	
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias	0		+2.0	Volts	
Input Impedance	3	5	7	kΩ	
RS-423 DRIVER					
TTL Input Levels					
V_{IL}	0		0.8	Volts	
V_{IH}	2.0			Volts	
Output					
HIGH Level Output	+3.6		+6.0	Volts	R_L=450Ω
LOW Level Output	–6.0		–3.6	Volts	R_L=450Ω

SPECIFICATIONS (Continued)

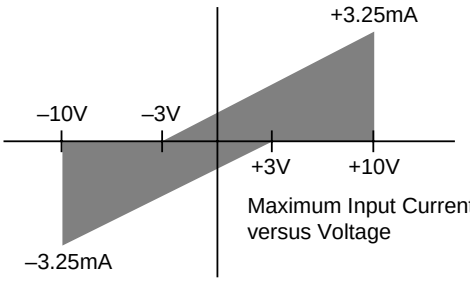
	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-423 DRIVER					
Open Circuit Voltage	±4.0		±9.0	Volts	
Short Circuit Current			±150	mA	
Power Off Current			±100	µA	
Transition Time			40	µs	Rise/fall time, 10-90%
Maximum Transmission Rate	120			kbps	
RS-423 RECEIVER					
TTL Output Levels					
V_{OL}	0		0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+12.0	Volts	
LOW Threshold	-7.0		-0.2	Volts	
Common Mode Range	-7.0		+12.0	Volts	
HIGH Input Current					Refer to graph
LOW Input Current					Refer to graph
Receiver Sensitivity			±0.2	Volts	
Input Impedance	4			kΩ	
POWER REQUIREMENTS					
V_{CC}	4.75		5.25	Volts	
I_{CC}		20	30	mA	V_{CC} =5V; no interface selected
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	-65		+150	°C	
Package		80–pin QFP			

RS422 RECEIVER



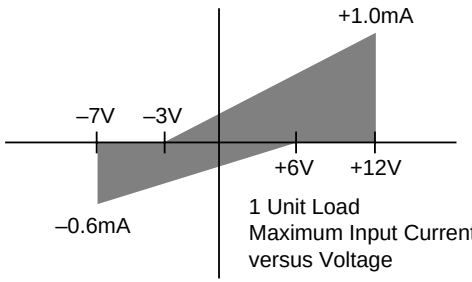
Maximum Input Current versus Voltage

RS423 RECEIVER



Maximum Input Current versus Voltage

RS485 RECEIVER



1 Unit Load
Maximum Input Current versus Voltage

AC CHARACTERISTICS

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
SINGLE–ENDED MODE					
RS-232					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		1.7		µs	Unloaded
t_{PLH}		1.1		µs	Unloaded
t_{PHL}		2.0	8.0	µs	Loaded with 3kΩ and 2,500pF
t_{PLH}		2.0	8.0	µs	Loaded with 3kΩ and 2,500pF
Receiver Propagation Delay					Input = 0V to 5.0V; 60kHz; Note 1
t_{PHL}			1.0	µs	
t_{PLH}			1.0	µs	
RS-423					
Driver Propagation Delay					Input = 0.8V to 2.0V; 60kHz
t_{PHL}		2.0	8.0	µs	Loaded with 450Ω
t_{PLH}		2.0	8.0	µs	Loaded with 450Ω
Receiver Propagation Delay					Input = -0.2V to 2.0V; ; 60kHz; Note 2
t_{PHL}			1.0	µs	
t_{PLH}			1.0	µs	
DIFFERENTIAL MODE					
RS-485					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz Note 3
t_{PHL}			200	ns	Loaded with 54Ω
t_{PLH}			200	ns	Loaded with 54Ω
Receiver Propagation Delay					Input = a to GND; B = -200mV to +200mV; 100kHz, Note 4
t_{PHL}			200	ns	
t_{PLH}			200	ns	
RS-422					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz Note 3
t_{PHL}			200	ns	Loaded with 100Ω
t_{PLH}			200	ns	Loaded with 100Ω
Receiver Propagation Delay					Input = a to GND; B = -200mV to +200mV; 100kHz, Note 4
t_{PHL}				ns	
t_{PLH}				ns	
V.35					
Driver Propagation Delay					Input = 0V to 3.0V; 100kHz Note 3
t_{PHL}			200	ns	Loaded with 100Ω
t_{PLH}			200	ns	Loaded with 100Ω
Receiver Propagation Delay					Input = a to GND; B = -200mV to +200mV; 100kHz, Note 4
t_{PHL}			200	ns	
t_{PLH}			200	ns	

OTHER AC CHARACTERISTICS (continued)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DELAY TIME FROM ENABLE MODE TO TRI–STATE MODE					
RS-232 (SINGLE–ENDED MODE)					
t_{PZL}; Enable to Output LOW		190		ns	3kΩ pull–up to output
t_{PZH}; Enable to Output HIGH		130		ns	3kΩ pull–down to output
t_{PLZ}; Disable from Output LOW		270		ns	5V to input
t_{PHZ}; Disable from Output HIGH		400		ns	GND to input
RS-422 (DIFFERENTIAL MODE)					
t_{PZL}; Enable to Output LOW		100		ns	3kΩ pull–up to output
t_{PZH}; Enable to Output HIGH		100		ns	3kΩ pull–down to output
t_{PLZ}; Disable from Output LOW		130		ns	5V to input
t_{PHZ}; Disable from Output HIGH		140		ns	GND to input

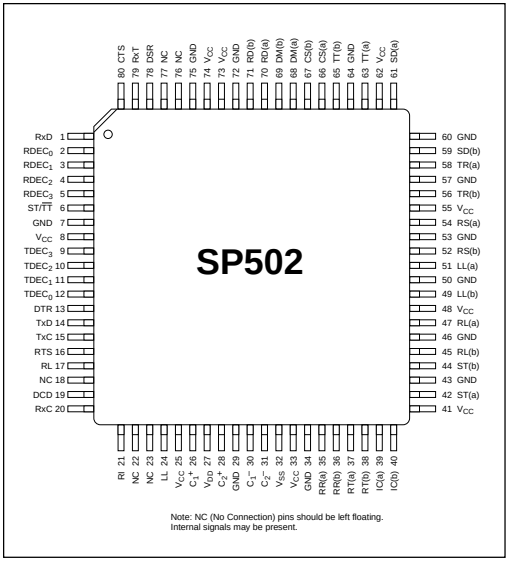
Notes:
1. Measured from 2.5V of R_{IN} to 2.5V of R_{OUT}.
2. Measured from one–half of R_{IN} to 2.5V of R_{OUT}.
3. Measured from 1.5V of T_{IN} to one–half of T_{OUT}.
4. Measured from 2.5V of R_O to 0V of A and B.

POWER MATRIX

Mode	Open Input	Input to 5V	Input to GND	AC Signal to Input	5V to Input with Load	GND to Input with Load	AC Signal with Load	Conditions
V.35 1110	20.71mA	21.5mA	20.74mA	28.32mA	58.19mA	55.64mA	73.08mA	With external driver output termination network; Input = 0.8V to 2V, 60kHz; Load = 3kΩ, 2500pF for RS-232; load = 100Ω for V.35
RS-232 0010	22.53mA	22.41mA	23.15mA	31.54mA	43.74mA	40.96mA	62.47mA	Input = 0.8V to 2V, 60kHz ; Load = 3kΩ, 2500pF
RS-422 0100	17.93mA	17.83mA	14.13mA	32.92mA	143.47mA	140.65mA	146.55mA	Input = 0.8V to 2V, 2.5MHz; Load = 100Ω
RS-485 0101	17.82mA	17.74mA	14.07mA	32.85mA	182.93mA	180.71mA	183.65mA	Input 0.8V to 2V, 2.5MHz; Load = 54Ω
RS-449 1100	19.93mA	19.87mA	17.84mA	23.57mA	134.90mA	131.35mA	131.94mA	Input = 0.8V to 2V, 60kHz; Load = 450Ω for RS-423; Load = 100Ω for RS-422
EIA-530 1101	19.85mA	19.83mA	17.82mA	23.54mA	134.90mA	131.25mA	131.78mA	Input = 0.8V to 2V, 60kHz; Load = 450Ω for RS-423; Load = 100Ω for RS-422

*All Driver Input Common V_{cc}=5V

PINOUT…



Note: NC (No Connection) pins should be left floating.
Internal signals may be present.

PIN ASSIGNMENTS…

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.
Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.
Pin 15 — TxC — Transmit Clock; common TTL input for both ST and TT driver outputs.
Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.
Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.
Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.
Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.
Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.
Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.
Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.
Pin 63 — TT(a) — Analog In or Out — Terminal Timing, inverted; sourced to TxC or RxT.
Pin 65 — TT(b) — Analog In or Out — Terminal Timing, non–inverted; sourced to TxC or RxT.
Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.
Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.
Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.
Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.
Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.
Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.
Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.
Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.
Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.
Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.
Pin 40 — IC(b)— Incoming Call; analog input, non-inverted; source for RI.
Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.
Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.
Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.
Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.
Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.
Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.
Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.
Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.
Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.
Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.
Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.
Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR.

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.
Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — RDEC0 – RDEC3 — Receiver decode register; configures receiver modes; TTL inputs.
Pin 6 — ST/$\overline{TT}$ — Enables ST or TT drivers, TTL input.
Pins 12–9 — TDEC0 – TDEC3 — Transmitter decode register; configures transmitter modes; TTL inputs.

POWER SUPPLIES
Pins 8, 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.
Pins 7, 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.
Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22µF, 16V.
Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.
Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.
Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES...

The **SP502** is a highly integrated serial transceiver that allows software control of its interface modes. The **SP502** offers hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, and EIA-530. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP502** is fabricated using low–power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin Quad FlatPack package.

The **SP502** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP502** has five (5) independent drivers and six (6) independent receivers and one half–duplex transceiver channel, which allows a maximum of six (6) drivers and seven (7) receivers. The driver and receiver configuration for the **SP502** is ideal for DTE applications. The **SP502** is made up of four separate circuit blocks – the charge pump, drivers, receivers, and decoder. Each of these circuit blocks is described in detail below.

THEORY OF OPERATION

Charge–Pump

The charge pump is a **Sipex** patented design (5,306,954) and uses a unique approach compared to older less efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. *Figure 3a* shows the waveform found on the positive side of capcitor C_2, and *Figure 3b* shows the negative side of capcitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

— V_{SS} charge storage —During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V to C_3. Simultaneously, the positive side of capaci-

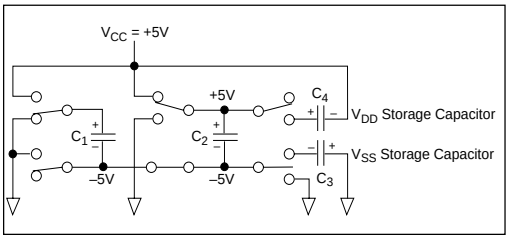


Figure 1. Charge Pump Phase 1.

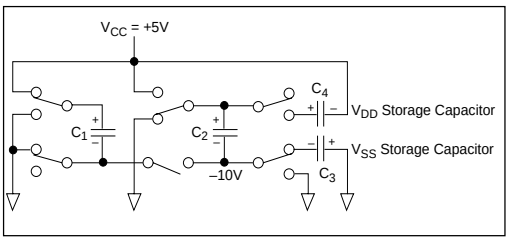


Figure 2. Charge Pump Phase 2.

tor C_1 is switched to +5V and the negative side is connected to ground.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V.

Phase 4

— V_{DD} transfer — The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated l0V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground, and the cycle begins again.

Since both V+ and V– are separately generated from V_{CC} in a no–load condition, V+ and V– will be symmetrical. Older charge pump approaches that generate V– from V+ will show a decrease in the magnitude of V– compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 22µF with a 16V breakdown rating. Two external Schottky diodes connected as in *Figure 6* are required for high rate of rise power supplies.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V– pins. The value of the external supply voltages must be no greater than ±l0V. The current drain for the ±10V supplies is used for RS-232, and RS-423 drivers. For the RS-232 driver the current requirement will be 3.5mA per driver, and for the RS-423 driver the worst case current drain will be 11mA per driver. The external

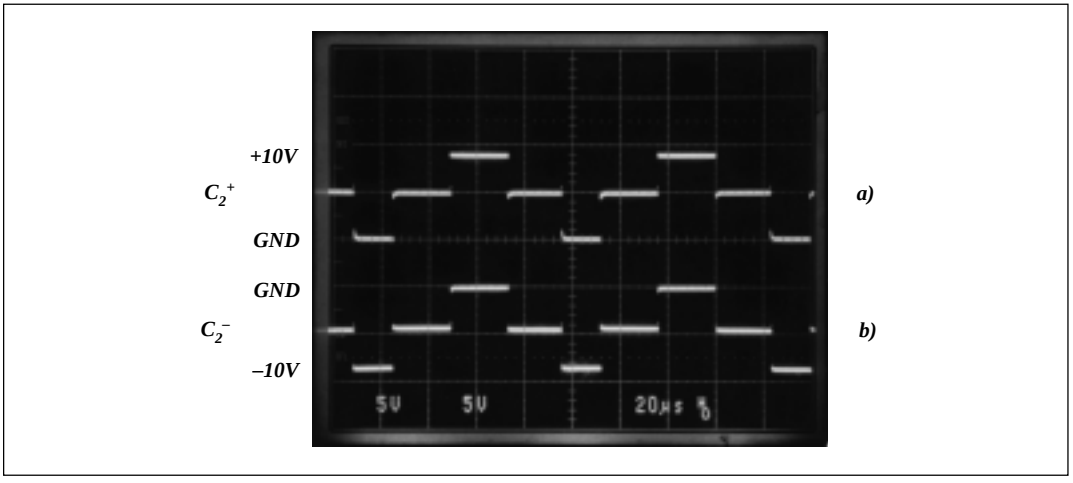


Figure 3. Charge Pump Waveforms

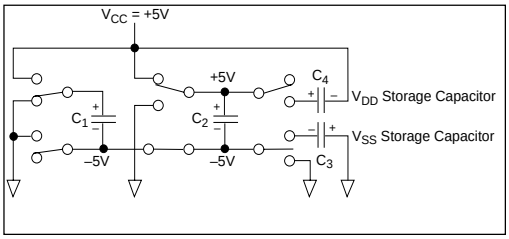


Figure 4. Charge Pump Phase 3.

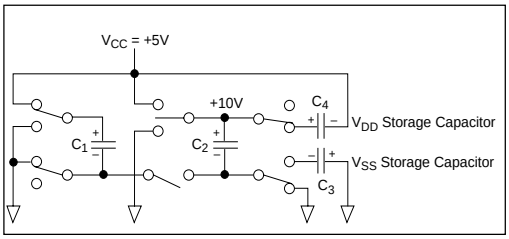


Figure 5. Charge Pump Phase 4.

power supplies should provide a power supply sequence of: +l0V, then +5V, followed by –l0V.

Drivers

The **SP502** has six (6) drivers which can be programmed in six different modes of operation. One of the drivers for the **SP502** is internally connected to an internal receiver input to make up a half-duplex configuration. As shown in the Mode Diagrams, the driver input of the half-duplex channel is shared with an adjacent driver such that when one is active the other is disabled.

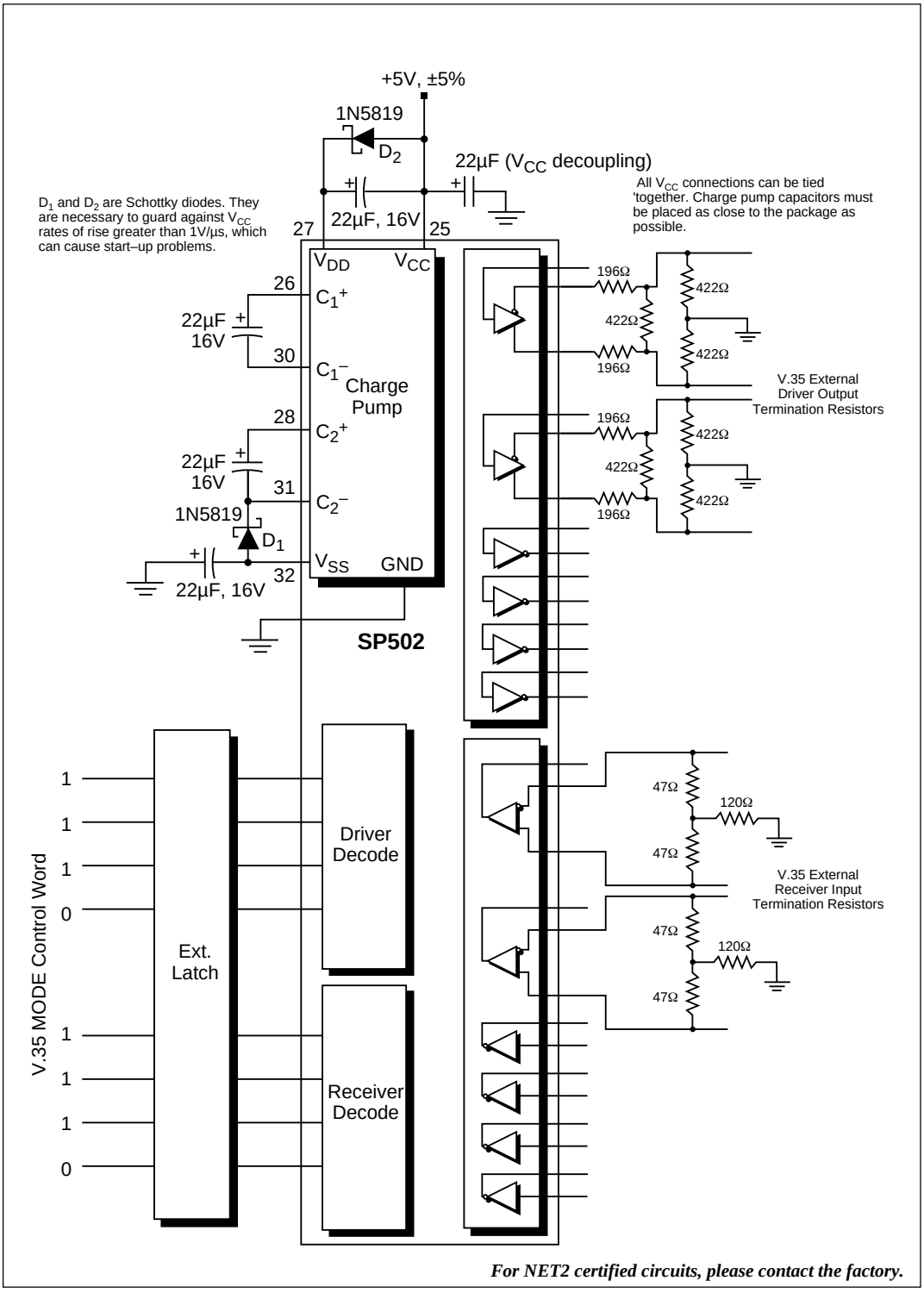
Control for the mode selection is done via a four–bit control word. The **SP502** does not have a latch; the control word must be externally latched either high or low to write the appropriate code into the **SP502**. The drivers are pre-arranged such that for each mode of operation the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows a summary of the electrical characteristics of the drivers in the different interface modes. Unused driver inputs can be left floating; however, to ensure a desired state with no input signal, pull–up resistors to +5V or pull–down resistors to ground are suggested. Since the driver inputs are both TTL or CMOS compatible, any value resistor less than 100kΩ will suffice.

There are three basic types of driver circuits — RS-232, RS-423, and RS-485. The RS-232 drivers output a minimum of ±5V level single–ended signals (with 3kΩ and 2500pF loading), and

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101
SD(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
SD(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TR(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
TR(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	RS-422+	RS-422+
RS(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
RS(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	RS-422+	RS-422+
RL(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
RL(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	tri–state	tri–state
LL(a)	tri–state	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
LL(b)	tri–state	tri–state	tri–state	RS-422+	RS-485+	tri–state	tri–state
ST(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
ST(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
TT(a)	tri–state	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
TT(b)	tri–state	tri–state	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

*The ST and TT driver outputs cannot be enabled simultaneously.

Table 1. SP502 Drivers



For NET2 certified circuits, please contact the factory.

Figure 6. Typical Operating Circuit

can operate up to 120kbps. The RS-232 drivers are used in RS-232 mode for all signals, and also in V.35 mode where they are used as the control line signals.

The RS-423 drivers output a minimum of ±3.6V level single–ended signals (with 450Ω loading) and can operate up to 120kbps. Open circuit V_{OL} and V_{OH} measurements may exceed the ±6V limitation of RS-423. The RS-423 drivers are used in RS-449 and EIA-530 modes as RL and LL outputs.

The third type of driver supports RS-485, which is a differential signal that can maintain ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS-485 drivers allow the drivers to also support RS-422 requirements of ±2V differential output levels with 100Ω loads. The RS-422 drivers are used in RS-449 and EIA-530 modes as clock, data, and some control line signals.

The RS-485–type drivers are also used in the V.35 mode. V.35 levels require ±0.55V signals with a load of 100Ω. In order to meet the voltage requirements of V.35, external series resistors with source impedance termination resistors must be implemented to voltage divide the driver outputs from 0 to +5V to 0 to +0.55V. *Figure 6* shows the values of the resistor network and how to connect them. The termination network also achieves the 50Ω to 150Ω source impedance for V.35. For applications that require V.11 signals for clock and data instead of V.35 levels, omit the external termination networks. All of the differential drivers, RS-485, RS-422, and V.35 can operate up to 5Mbps.

Receivers

The **SP502** is equipped with seven (7) receivers which can be programmed in six (6) different modes of operation. One of the seven (7) receivers (RxT) is part of a half-duplex channel, which means its inputs are shared with a driver output, as shown in the Mode Diagrams. The RxT receiver has its inputs internally connected to the TT(a) and TT(b) pins. The select pin labeled ST/TT enables either the TT-driver or the ST-driver, but it does not disable the receiver. The RxT receiver is always connected to the TT(a) and TT(b) pins. Any signal that is received or transmitted on TT(a) and TT(b) will trigger a TTL-output at the RxT pin.

Control for the mode selection is done via a 4–bit control word that is independent from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed,

Pin Label	Mode:	RS-232	V.35	RS-422	RS-485	RS-449	EIA-530
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101
RD(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
RD(b)	Undefined	15kΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
RT(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
RT(b)	Undefined	15kΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+
CS(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
CS(b)	Undefined	15kΩ to GND	15kΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
DM(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
DM(b)	Undefined	15kΩ to GND	15kΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
RR(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-422–	RS-422–
RR(b)	Undefined	15kΩ to GND	15kΩ to GND	RS-422+	RS-485+	RS-422+	RS-422+
IC(a)	Undefined	RS-232	RS-232	RS-422–	RS-485–	RS-423	RS-423
IC(b)	Undefined	15kΩ to GND	15kΩ to GND	RS-422+	RS-485+	15kΩ to GND	15kΩ to GND
SCT(a)	Undefined	RS-232	V.35–	RS-422–	RS-485–	RS-422–	RS-422–
SCT(b)	Undefined	15kΩ to GND	V.35+	RS-422+	RS-485+	RS-422+	RS-422+

*TT(a) and TT(b) can be programmed as driver outputs or receiver inputs.

Table 2. SP502 Receivers

the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows a summary of the electrical characteristics of the receivers in the different interface modes. Unused receiver inputs can be left floating without causing oscillation. To ensure a desired state of the receiver output, a pull–up resistor of 100kΩ to +5V should be connected to the inverting input for a logic LOW, or the non–inverting input for a logic high. For single-ended receivers, a pull–down resistor to ground of 5kΩ is internally connected, which will ensure a logic HIGH output.

There are three basic types of receivers — RS-232, RS-423, and RS-485. The RS-232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120kbps. RS-232 receivers are used in RS-232 mode for all signal types, and in V.35 mode for control line signals.

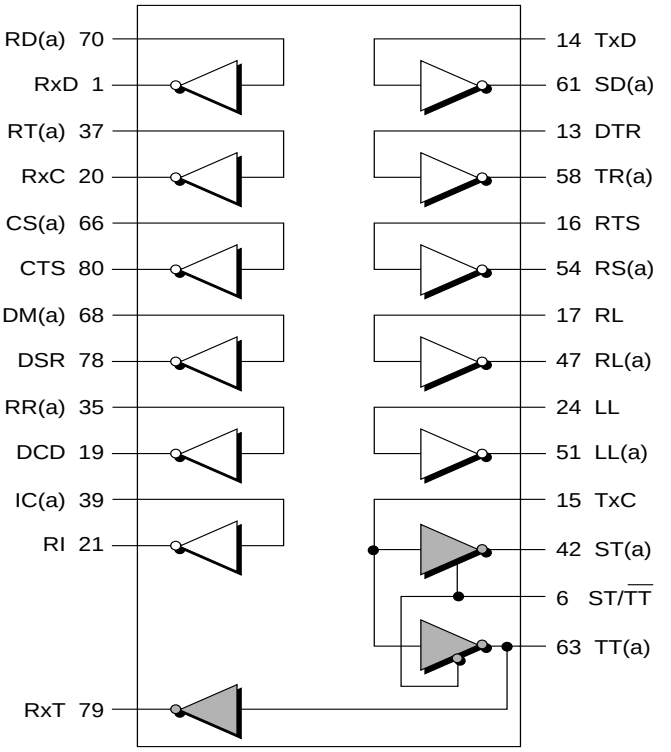
The RS-423 receivers are also single–ended but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4kΩ, with an operating voltage range of ±7V. The RS-423 receivers can operate up to 120kbps. RS-423 receivers are used for the IC signal in RS-449 and EIA-530 modes, as shown in *Table 2*.

The third type of receiver supports RS-485, which is a differential interface mode. The RS-485 receiver has an input impedance of 15kΩ and a differential threshold of ±200mV. Since the characteristics of an RS-422 receiver are actually subsets of RS-485, the receivers for RS-422 requirements are identical to the RS-485 receivers. RS-422 receivers are used in RS-449 and EIA-530 for receiving clock, data, and some control line signals. The RS-485 receivers are also used for the V.35 mode. V.35 levels require the ±0.55V signals with a load of 100Ω. In order to meet the V.35 input impedance of 100Ω, the external termination network of *Figure 6* must be applied. The threshold of the V.35 receiver is ±200mV. The V.35 receivers can operate up to 5Mbps. All of the differential receivers can receive data up to 5Mbps.

Decoder

The **SP502** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP502**. Undefined codes may represent other interface modes not specified or random outputs (consult the factory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. The drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs in an undetermined state. All receivers, with the exception of SCT, do not have tri-state capability; the outputs will either be HIGH or LOW depending upon the state of the receiver input.

MODE: RS-232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



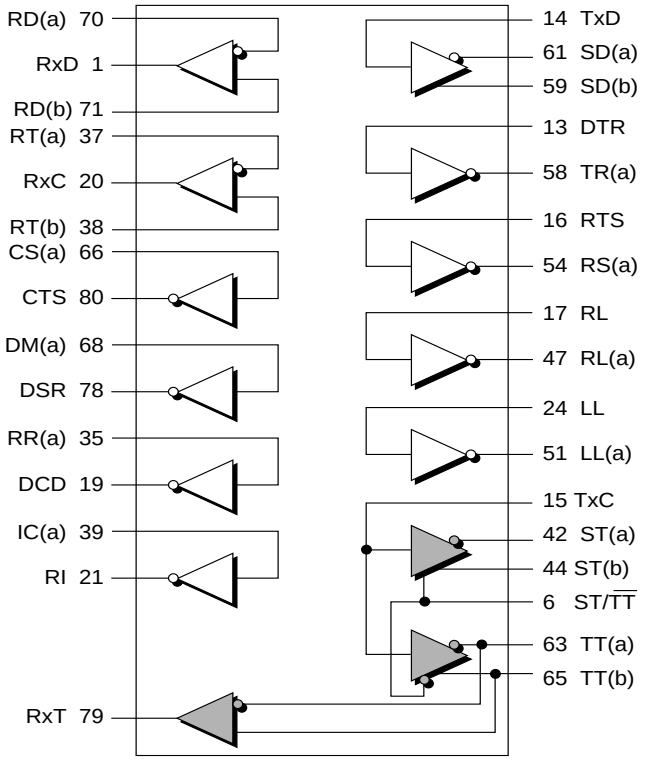
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 7. Mode Diagram — RS-232

MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



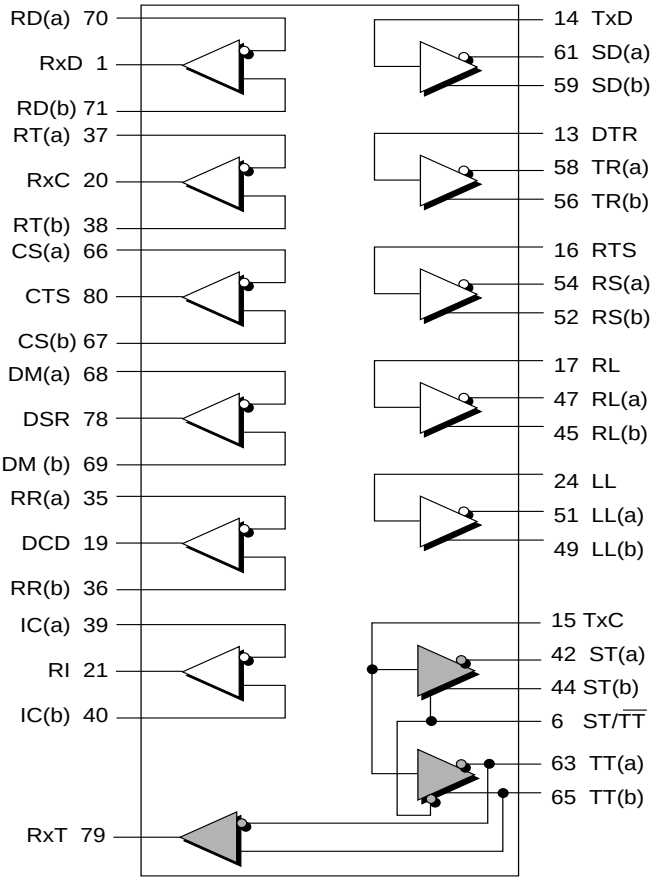
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 8. Mode Diagram — V.35

MODE: RS-422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



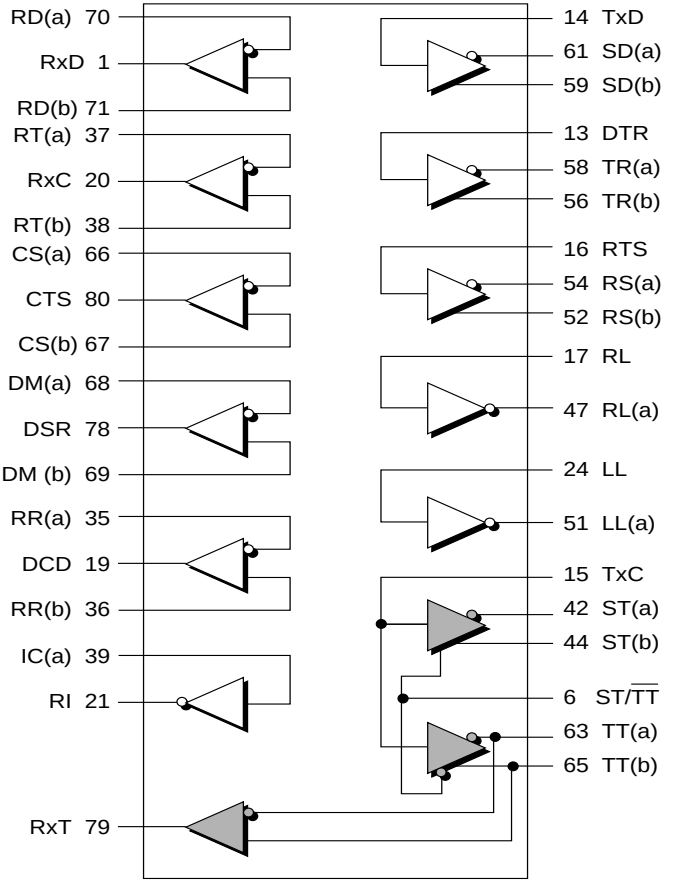
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 9. Mode Diagram — RS-422

MODE: RS-449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



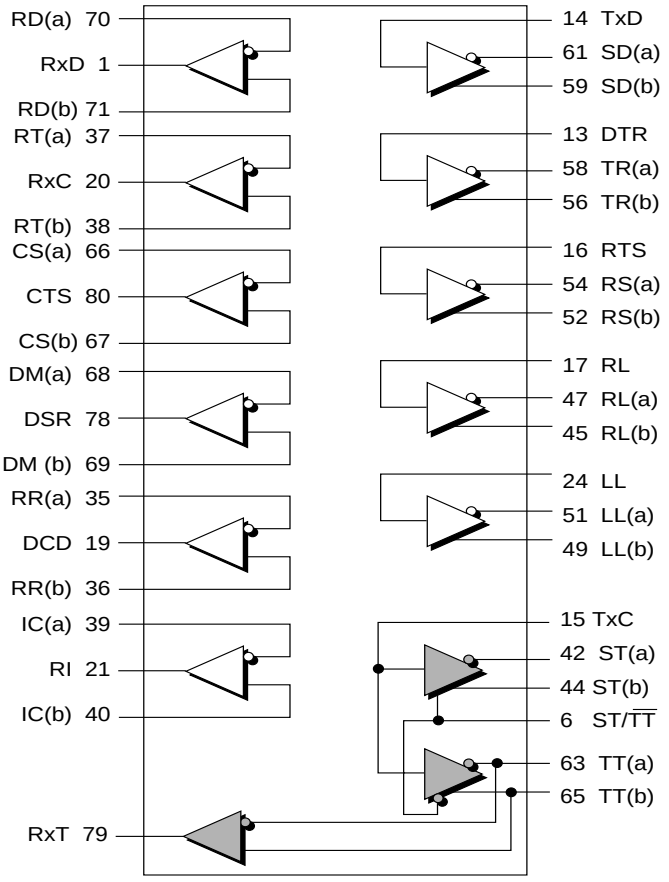
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 10. Mode Diagram — RS-449

MODE: RS-485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



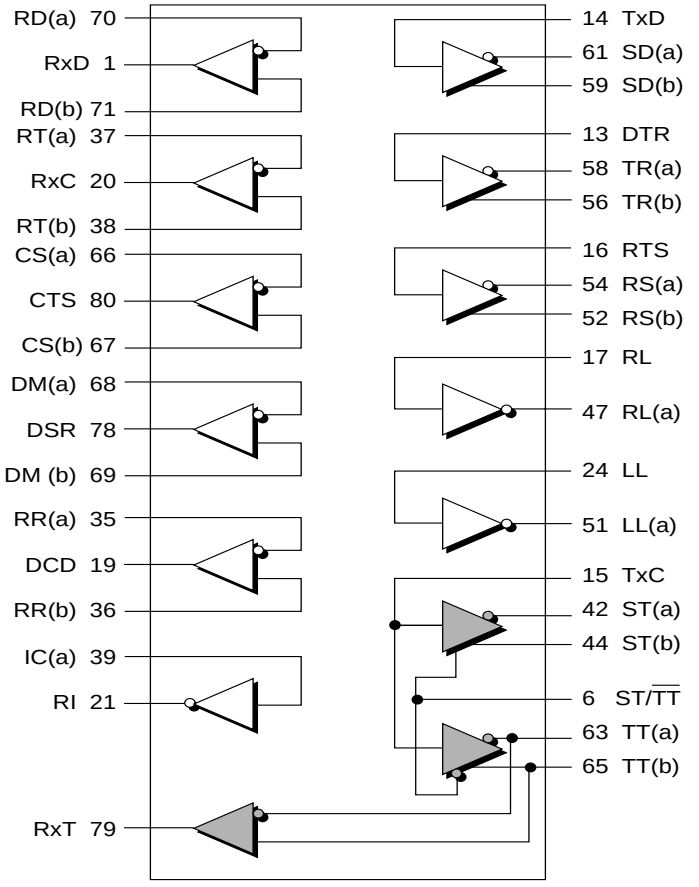
ST/$\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 11. Mode Diagram — RS-485

MODE: EIA-530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



$ST/\overline{TT}$	ST	TT	RxT*
1	Enabled	Disabled	Active
0	Disabled	Enabled	Inactive

* TT driver must be disabled to allow TT(a) and TT(b) to serve as receiver inputs.

* When the RxT receiver is active, TT(a) and TT(b) act as receiver inputs. When the RxT receiver is inactive, it cannot serve as a receiver since its inputs are internally connected to the TT(a) and TT(b) driver outputs.

Figure 12. Mode Diagram — EIA-530

APPLICATION EXAMPLE

The example application that follows is a fully configured serial I/O channel in a DTE configuration. The example is comprised of the following functional elements:

- Processor
- SCC
- **SP502**
- Mode Select Register (R0[WR])
- RL & LL Control Bit Register (R1[WR])
- RI Status Bit Register (R1[RD])
- Address Decode Logic
- Baud Rate Clock Source
- I/O Connector Interface

Each of the elements of the application example are described below. Please refer to *Figure13*.

Processor

The example schematic shows a generic 8-bit processor connected to a generic SCC. The processor is also connected to three registers. The registers are described in further detail below.

Address Decode Logic

The address decode logic is connected to the Processor control and address busses and provides the logic necessary to decode the I/O read and write operations for the SCC, Mode Select Register, RL and LL Control Bit Register and the RI Status Bit Register.

SCC

The SCC provides the I/O functions for a single serial channel. The SCC is connected to the Processor I/O bus and is programmed by the user software. The SCC's TTL-level serial I/O pins are connected to the corresponding TTL-level serial I/O pins on the **SP502**.

SP502

The **SP502** provides buffering and translation from TTL levels to the selected physical level interface standard, such as RS-232, V.35, etc. The physical level interface pins are connected to a standard 25 pin D-subminiature connector wired in a DTE configuration with the pin assignments corresponding to the EIA-530 specification. This choice was purely arbitrary. However, it provides all the necessary signals to support standards other than EIA-530, such as V.35, RS-232, RS-449, etc. with an appropriate cable adapter.

The **SP502** driver and receiver modes are independently configured by programming the **SP502**'s RDEC and TDEC input pins. In the example, the pins are driven by the Mode Select Register with a programmed value stored by the user's software.

Since the **SP502** is shown in a DTE configuration, the example assumes that any synchronous interface clocking will be provided by the attached DCE device. Consequently, the ST/TT pin is tied to +5V, thus causing the **SP502** to receive the transmit clock on the TT(a) and TT(b) input pins and output the transmit clock to the SCC on the RxT output pin. The receive clock is input to the **SP502** on the RT(a) and RT(b) pins and output to the SCC on the RxC pin.

Mode Select Register

The mode select register is an 8-bit latch attached to the Processor data bus. The Processor, under user-software control, can program the Mode Select Register with the appropriate values to select the **SP502**'s driver and receiver modes.

The table shown on the schematic below the register lists the values for programming the register to drive the RDEC and TDEC pins on the **SP502** for the desired physical level interface. The receivers and drivers can be programmed independently, but in this example the Mode Select Register must be programmed with both the RDEC and TDEC values at the same time. This is because the RDEC and TDEC pins are driven from the same 8-bit latch.

Note that selecting modes for TDEC that are shown in the table as undefined will result in the drivers operating in an undefined mode and should not be used. Likewise, selecting modes for RDEC that are shown in the table as undefined will result in indeterminate logic levels present on the TTL outputs of the **SP502**. Undefined RDEC or TDEC values should never be programmed.

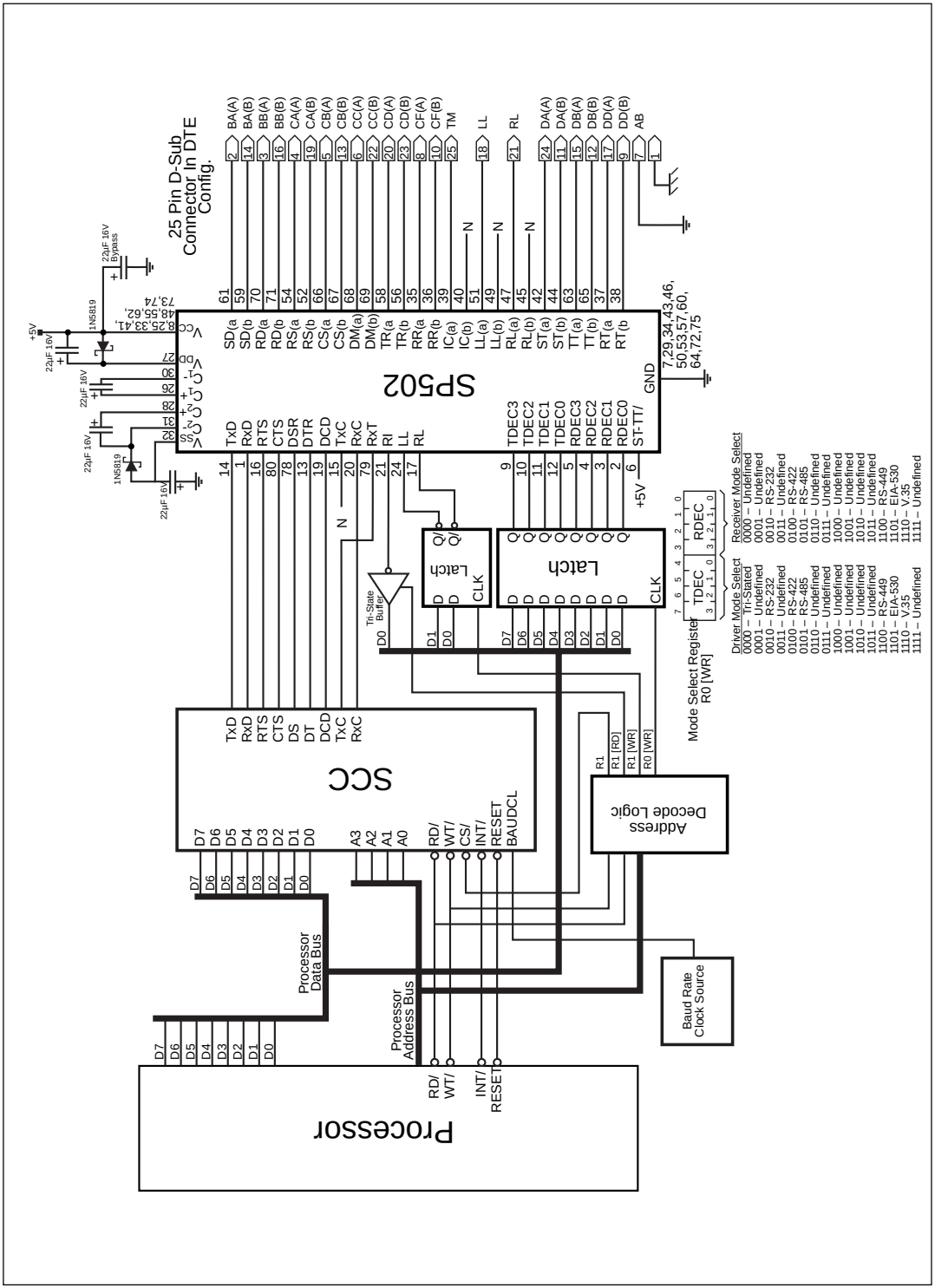


Figure 13. DTE Serial Communications Channel

Several other approaches for driving the RDEC and TDEC signals are possible. One approach would use two independent 4-bit latches, one each to drive the RDEC and TDEC pins as separate groups. Another approach would use one 4-bit latch, each output of the latch would drive a corresponding pair of RDEC/TDEC signals. For instance, $RDEC_0$ and $TDEC_0$ could be tied together and be driven by the low order bit of the 4-bit latch.

RL & LL Control Bit Registers

A 2-bit latch is used to allow the Processor to program the states of the RL and LL interface signals. This latch is necessary since most SCCs do not support RL and LL control signals.

RI Status Bit Register

A 1-bit read register is implemented using a tri-state buffer. This will allow the Processor to read the state of the **RI** (Ring Indicator) interface signal. This is necessary since most SCCs do not support the **RI** interface signal.

The example interface shows the **SP502A**'s IC(a) input tied to the EIA-530 signal TM (Test Mode). EIA530 does not specify an **RI** signal. If EIA-530 operation is required, the **RI** Status Bit Register could be used to monitor the condition of the TM signal or it could be ignored. For other interface standards, the connector pin 25 on the schematic could be tied to the **RI** signal through a cable adapter arrangement. For instance, if RS-232 operation is used, pin 25 of the connector could be tied to pin 22 of the RS-232 adapter (circuit CE) and the **RI** Status Bit Register then used to monitor the RS-232 signal for ring indicator.

Baud Rate Clock Source

Most SCCs require an external clock source for operation in asynchronous and self-clocking applications.

I/O Connector Interface

The I/O connector is wired to the **SP502A** such that the interface represents a DTE device. As shown, the connector is wired in an EIA-530 configuration with EIA-530 signal mnemonics. A 25-pin connector wired to the EIA-530 specification provides pins for all interface signals supported by the **SP502**. If the **SP502** is programmed for other physical interfaces, such as V.35, then an adapter cable will provide the necessary conversion from the EIA-530 pin-outs to those required by the V.35 standard together with its ISO-2593 connector.

Notes Regarding V.35 Operation

The user will have to provide additional resistor networks if correct V.35 signal levels and termination impedances are required. This is necessary because the **SP502** does not provide V.35 signal terminations when programmed for V.35 operation. Two approaches are possible. First, if the **SP502** is permanently programmed to operate as V.35 only, with no other interface standard required, then the appropriate resistors can be mounted on the PCB near the **SP502**. Second, if the **SP502** will be programmed for a variety of standards, then a better approach might be to provide the resistors as part of the cable adapter assembly used to convert from the standard EIA-530 connector pin-outs shown in the example to the V.35/ISO-2593 connector and pin-outs.

SP502/SP503 EVALUATION BOARD

The **SP502/SP503 Evaluation Board** (EB) Is designed to offer as much flexibility to the user as possible. Each board comes equipped with an 80-pin QFP Zero-Insertion Force socket to allow for testing of multiple devices. The control lines and inputs and outputs of the device can be controlled either manually or via a data bus under software control. There is a 50-pin connector to allow for easy connection to an existing system via ribbon cable. There are also open areas on the PC board to add additional circuitry to support application-specific requirements.

Manual Control

The SP502/SP503EB will support both the **SP502** or **SP503** multi-mode serial transceivers. When used for the **SP502,** disregard all notation on the board that is in [brackets] . The **SP502** has a half-duplex connection between the RxT receiver and the TT driver. Due to this internal connection, the RxT receiver inputs can be accessed via the TT(a) and TT(b) pins. If the user needs separate receiver input test pins, jumpers JP1 and JP2 can be inserted to allow for separate receiver inputs located at SCT(a) and SCT(b). The corresponding TTL output for this receiver is labeled as SCT. This test point is tied to pin 79 of the **SP502** or **SP503**. Pin 7 of the evaluation board is connected to the DIP switch, and is labeled as (SCTEN). When used with the **SP502**, this pin should be switched to a low state. When the evaluation board is used with the **SP503**, pin 7 is a tri-state control pin for the SCT receiver.

The transceiver I/O lines are brought out to test pins arranged in the same configuration as shown elsewhere in this data sheet. A top layer silk-screen shows the drivers and receivers to allow direct correlation to the data sheet. The transmitter and receiver decode bits are tied together and are brought out to a DIP switch for manual control of both the driver and receiver interface modes. Since the coding for the drivers and receivers is identical, the bits have been tied together. The DIP switch has 7 positions, four of which are reserved for the TDEC/RDEC control. The other three are used as tri-state control pins. The labels that are in [brackets] apply only to the **SP503**. If a logic one is asserted, the corresponding red LED will be lit. If a zero is asserted, the corresponding red LED will not be lit.

Software Control

A 50-pin connector brings all the analog and digital I/O lines, V_{CC}, and GND to the edge of the card. This can be wired to the user's existing design via ribbon cable. The pinout for the connector is described in the following section. When the evaluation board is operated under software control, the DlP switch should be set up so that all bits are LOW (all LEDs off). This will tie pull-down resistors from the inputs to ground and let the external system control the state of the control inputs.

Power and Ground Requirements

The evaluation board layout has been optimized for performance by using basic analog circuit techniques, The four charge-pump capacitors must be 22µF (16V) and be placed as close to the unit as possible; tantalum capacitors are suggested. The decoupling capacitor must be a minimum of 1µF; depending upon the operating environment, 10µF should be enough for worst case situations. The ground plane for the part must be solid, extending completely under the package. The power supplies for the device should be as accurate as possible; for rated performance ±5% is necessary. The power supply current will vary depending upon the selected mode, the amount of loading and the data rate. As a maximum, the user should reserve 200mA for I_{CC}. The worst-case operating mode is RS-485 under full load of six (6) drivers supplying 1.6V to 54Ω loads. The power and ground inputs can be supplied through either the banana jacks on the evaluation board (Red = V_{CC} = +5V±5%; Black = GND) or through the connector.

For reference, the 80-pin QFP Socket is a TESCO part number FPQ-80-65-09A. The 50-pin connector is an AMP part number 749075-5.

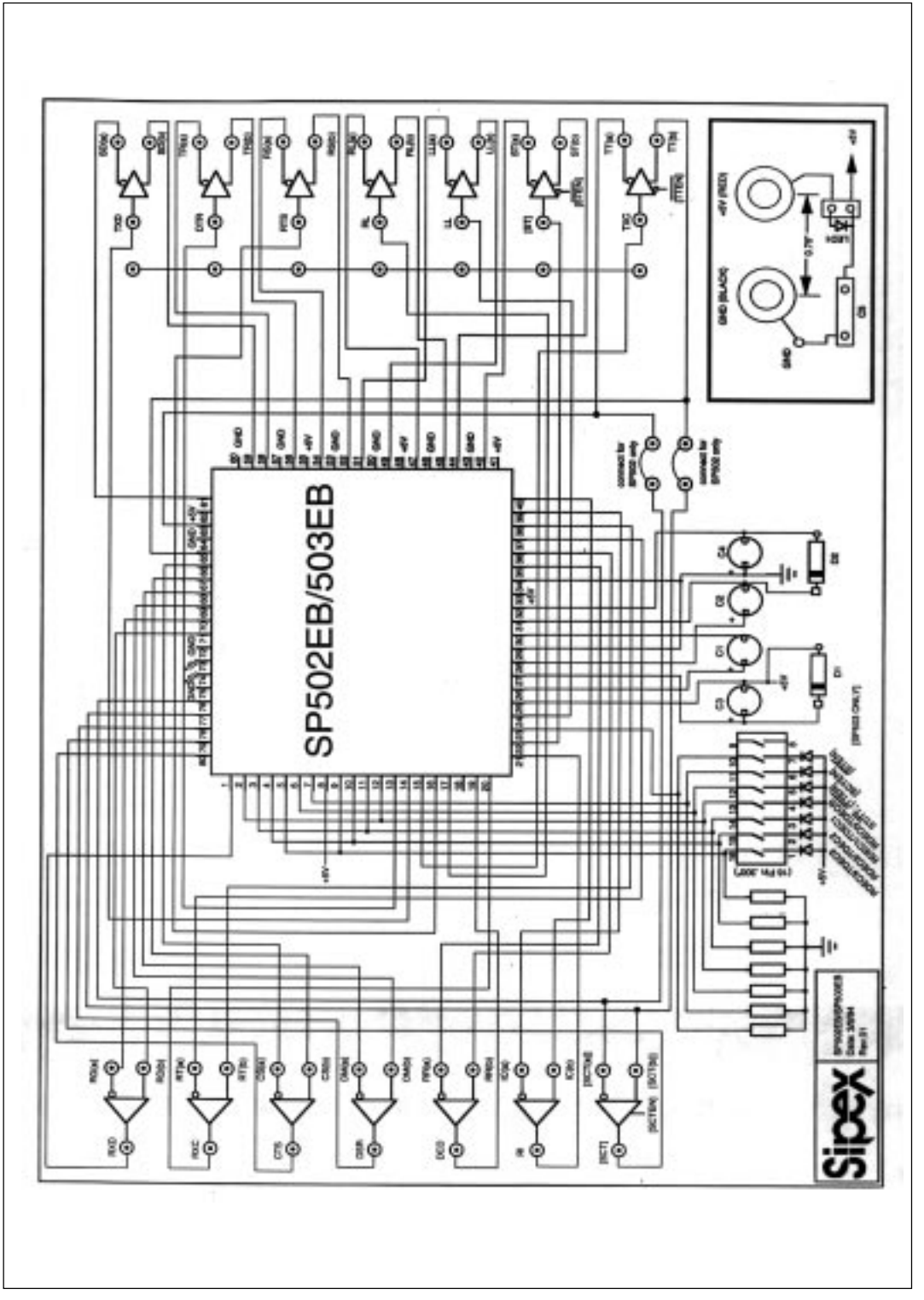


Figure 13. SP502/503 Evaluation Board Schematic

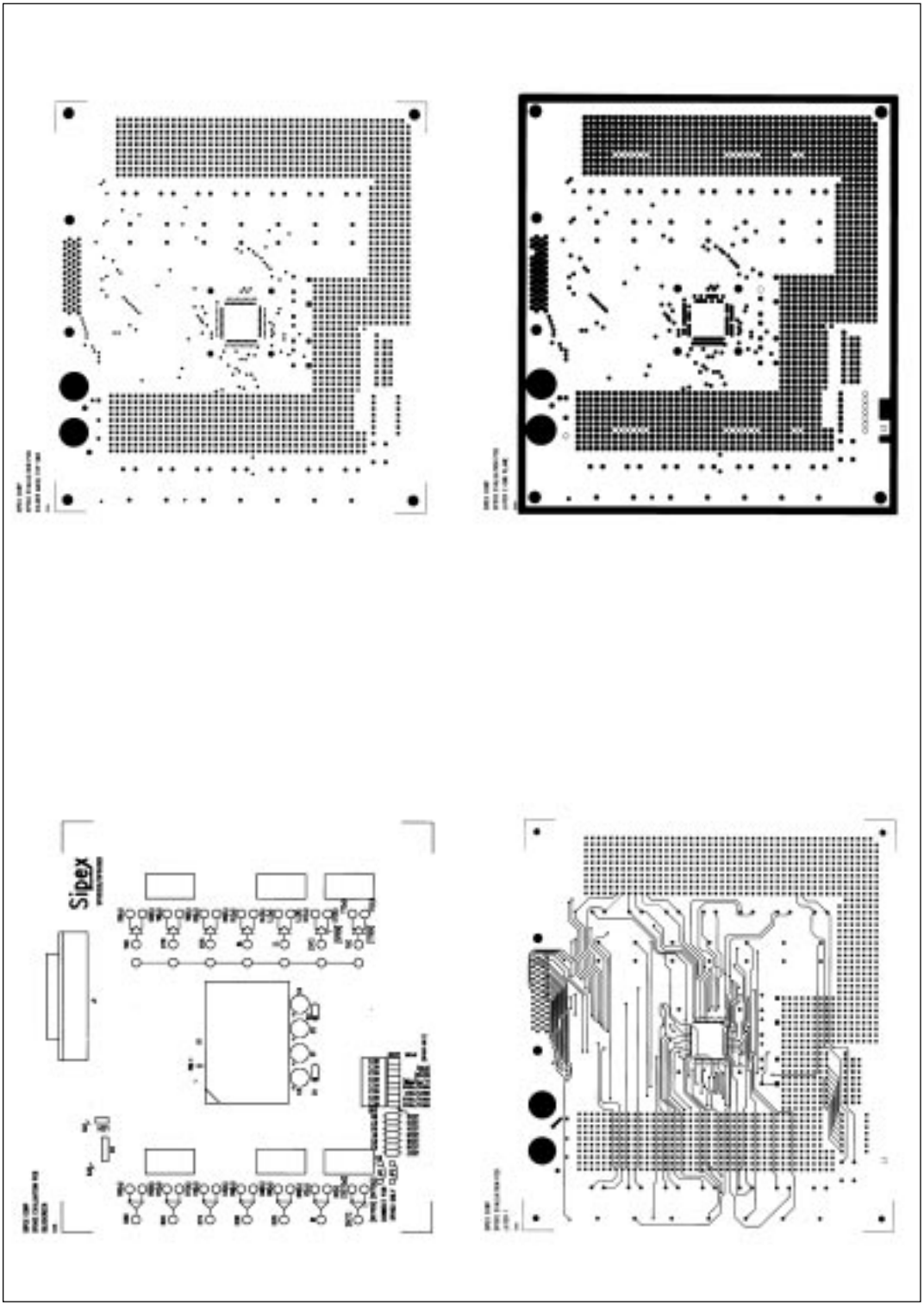


Figure 14a. Evaluation Board — Top Layers

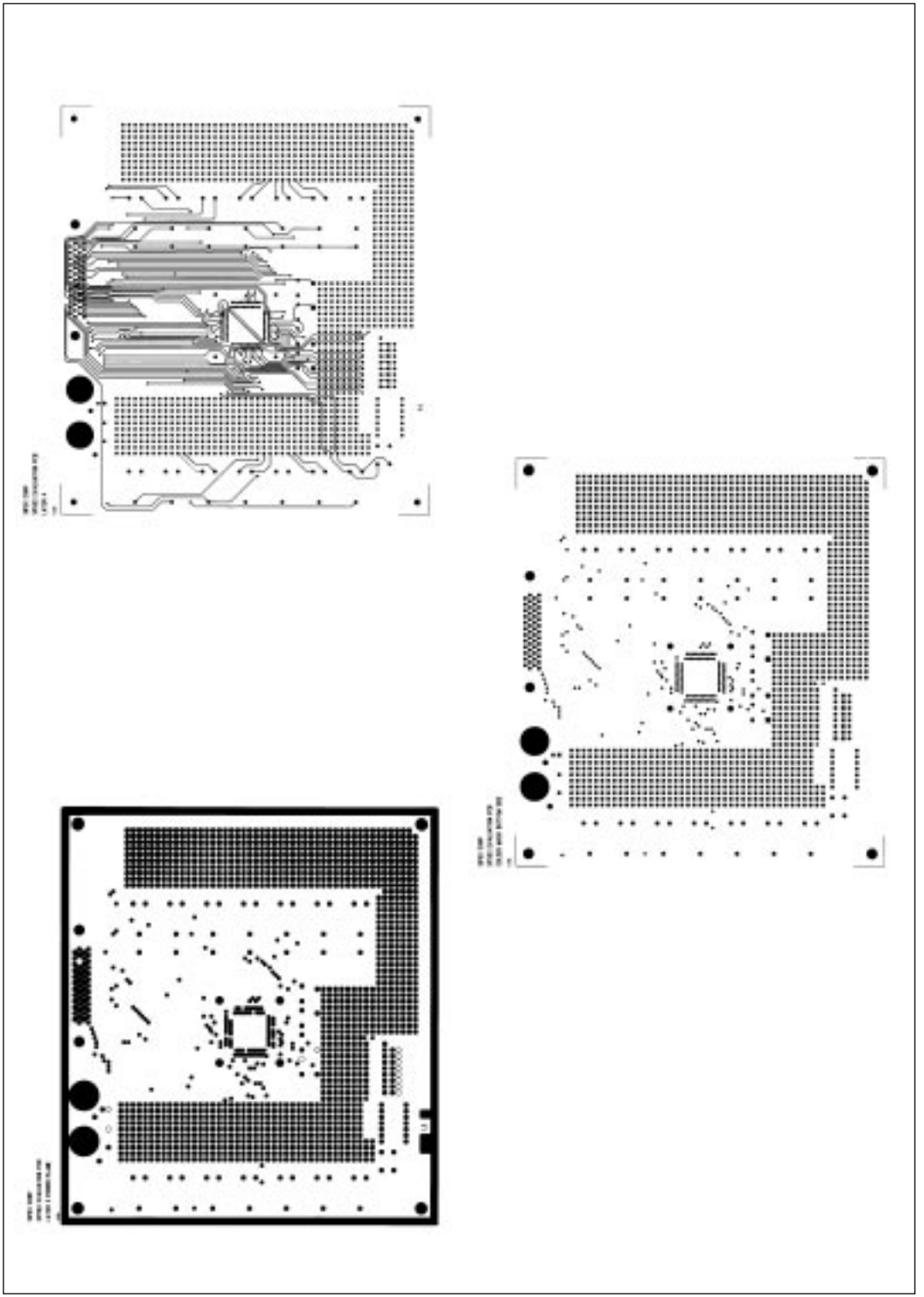


Figure 14b. Evaluation Board — Bottom Layers

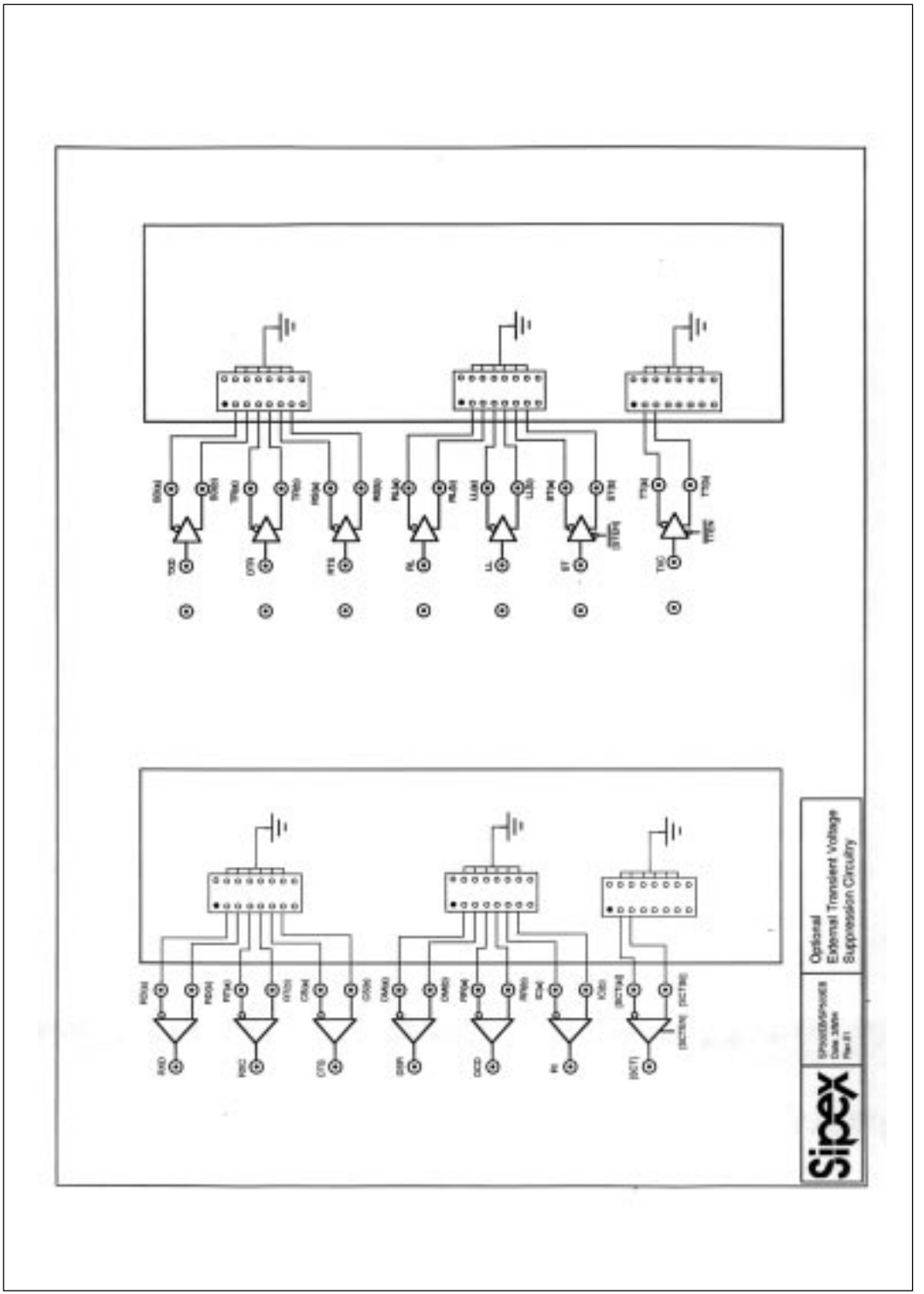
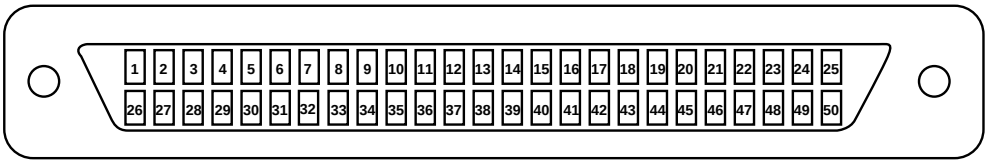
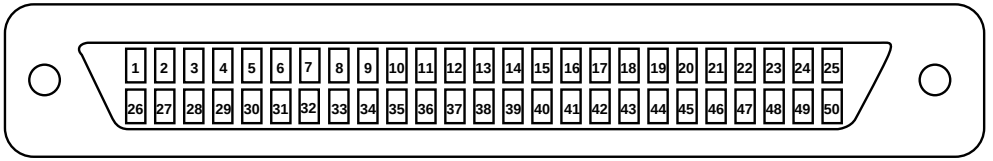


Figure 15. External Transient Suppressors



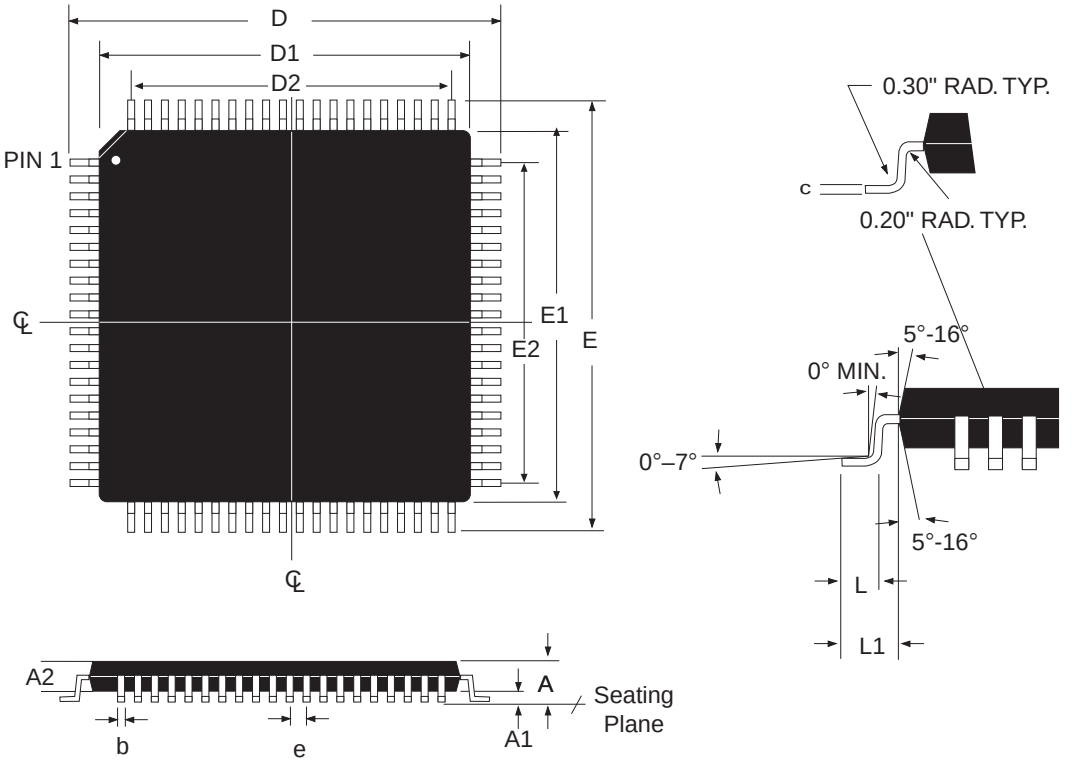
EDGE CONNECTOR	DUT PIN DESCRIPTIONS
01	TxD (pin 14) –TTL Input – Transmit data; source for SD(a) and SD(b) outputs.
02	DTR (pin 13) – TTL Input – Data terminal ready: source for TR(a) and TR(b) outputs.
03	ST/$\overline{TT}$ (pin 6) –TTL Input – ST/$\overline{TT}$ select pin; enables ST drivers and disables TT drivers when high. Disables ST drivers and enables TT drivers when low.
04	DEC_3/$RDEC_3$ (pin 5) – TTL Input – Transmitter/Receiver decode register.
05	$TDEC_2$/$RDEC_2$ (pin 4) – TTL Input – Transmitter/Receiver decode register.
06	$TDEC_1$/$RDEC_1$ (pin 3) – TTL Input – Transmitter/Receiver decode register.
07	$TDEC_0$/$RDEC_0$ (pin 2) – TTL Input – Transmitter/Receiver decode register.
08	RxD (pin 1) – TTL Output – Receive data; sourced from RD(a) and RD)b) inputs.
09	CTS (pin 80) – TTL Output – Clear to send; sourced from CS(a) and CS(b) inputs.
10	RxT (pin 79) – TTL Output – RxT; sourced from TT(a), TT(b) inputs.
11	DSR (pin 78) – TTL Output – Data set ready; sourced from DM(a) and DM(b) inputs.
12	RD(b) (pin 71) – Analog In – Receive data, non–inverted; source for RxD.
13	RD(a) (pin 70) – Analog In – Receive data, inverted: source for RxD.
14	DM(b) (pin 69) – Analog In – Data mode, non–inverted; source for DSR.
l5	DM(a) (pin 68) – Analog In – Data mode, inverted; source for DSR.
16	CS(b) (pin 67) – Analog In – Clear to send; non–inverted; source for CTS.
17	CS(a) (pin 66) – Analog In – Clear to send, inverted; source for CTS.
18	TT(b) (pin 65) – Analog Out – Terminal timing, non–inverted: sourced from TxC input.
19	TT(a) (pin 63) – Analog Out – Terminal timing; inverted: sourced from TxC input.
20	TR(a) (pin 58) – Analog Out – Terminal ready, inverted; sourced from DTR.
21	TR(b) (pin 56) – Analog Out – Terminal ready; non–inverted; sourced from DTR.
22	SD(a) (pin 61) – Analog Out – Send data, inverted; sourced from TxD.
23	SD(b) (pin 59) – Analog Out – Send data; non–inverted; sourced from TxD.
24	RS(a) (pin 54) – Analog Out – Ready to send; inverted; sourced from RTS.
25	RS(b) (pin 52) – Analog Out – Ready to send, non–inverted; sourced from RTS.



EDGE CONNECTOR	DUT PIN DESCRIPTIONS
26	ST (pin 22) – TTL Input – Send Timing; source for ST(a) and ST(b) outputs. SP503 only.
27	$\overline{\text{STEN}}$ (pin 23) – TTL Input — Driver enable control pin; active low. SP503 only,
28	SCT(a) (pin 76) – Analog Input – Inverting; input for SCT receiver; SP503 only.
29	SCT(b) (pin 77) – Analog Input – Non–inverting; input for SCT receiver. SP503 only.
30	V_{CC} — +5V for all circuitry.
31	GND — signal and power ground.
32	LL(a) (pin 51) – Analog Out – Local loopback, inverted; sourced from LL.
33	LL(b) (pin 49) – Analog Out – Local loopback, non–inverted sourced from LL.
34	RL(a) (pin 47) – Analog Out – Remote loopback; inverted; sourced from RL.
35	RL(b) (pin 45) – Analog Out – Remote loopback; non–inverted; sourced from RL.
36	ST(b) (pin 44) – Analog Out – Send timing, non–inverted; sourced from TxC.
37	ST(a) (pin 42) – Analog Output –Send timing, inverted; sourced from TxC.
38	IC(b) (pin 40) – Analog In – Incoming call; non–inverted; source for Rl.

EDGE CONNECTOR	DUT PIN DESCRIPTIONS
39	IC(a) (pin 39) – Analog In – Incoming call; inverted; source for Rl.
40	RT(b) (pin 38) – Analog In – Receive timing, non–inverted; source for RxC.
41	RT(a) (pin 37) – Analog In – Receive timing; inverted; source from RxC.
42	RR(b) (pin 36) – Analog In – Receiver ready; non–inverted; source for DCD.
43	RR(a) (pin 35) – Analog In – Receiver ready; inverted; source for DCD.
44	LL (pin 24) – TTL Input – Local loopback; source for LL(a) and LL(b) outputs.
45	Rl (pin 21) – TTL Output – Ring indicator; sourced from IC(a) and IC(b) inputs.
46	RxC (pin 20) – TTL Output – Receive clock; sourced from RT(a) and RT(b) inputs.
47	DCD (pin 19) – TTL Output – Data carrier detect; sourced from RR(a) and RR(b) inputs.
48	RL (pin 17) – Analog Out – Remote loopback; source for RL(a) and RL(b) outputs.
49	RTS (pin 16) – TTL Input – Ready to send; source for RS(a) and RS(b) outputs.
50	TxC (pin 15) – TTL Input – Transmit clock; source for TT(A) and TT(B) outputs.

PACKAGE: 80 PIN MQFP

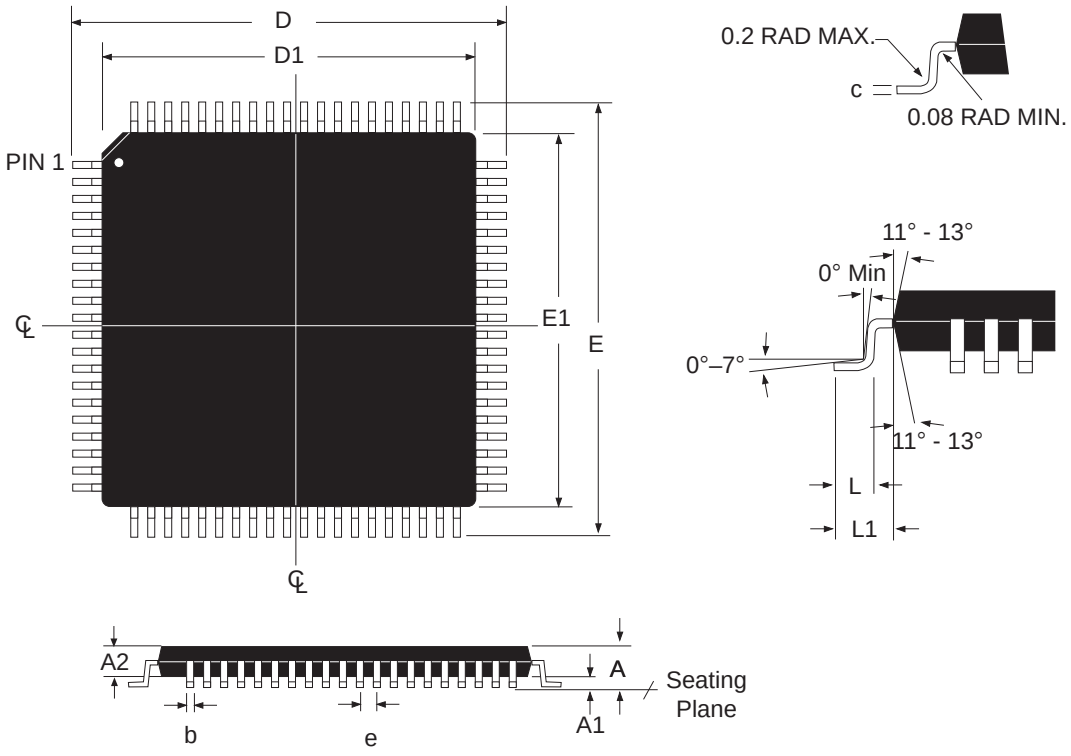


DIMENSIONS Minimum/Maximum (mm)	80–PIN MQFP JEDEC MS-22 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			2.45
A1	0.00		0.25
A2	1.80	2.00	2.20
b	0.22		0.40
D	17.20 BSC		
D1	14.00 BSC		
D2	12.35 REF		
E	17.20 BSC		
E1	14.00 BSC		
E2	12.35 REF		
e	0.65 BSC		
N	80		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.73	0.88	1.03
L1	1.60 BASIC		

80 PIN MQFP (MS-022 BC)

PACKAGE: 80 PIN LQFP



DIMENSIONS Minimum/Maximum (mm)	80-PIN LQFP JEDEC MS-026 (BEC) Variation		
SYMBOL	MIN	NOM	MAX
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.22	0.32	0.38
D	16.00 BSC		
D1	14.00 BSC		
e	0.65 BSC		
E	16.00 BSC		
E1	14.00 BSC		
N	80		

COMMON DIMENTIONS			
SYMBL	MIN	NOM	MAX
c	0.11		23.00
L	0.45	0.60	0.75
L1	1.00 BASIC		

80 PIN LQFP

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP502CF	0°C to +70°C	80–pin JEDEC (MS-022 BC) MQFP
SP502CM	0°C to +70°C	80-pin JEDEC (MS-026 BEC) LQFP

Sipex Corporation

ANALOG EXCELLENCE

Sipex Corporation

Headquarters and Sales Office
233 South Hillview Drive
Milpitas, CA 95035
TEL: (408) 934-7500
FAX: (408) 935-7600

Sales Office
22 Linnell Circle
Billerica, MA 01821
TEL: (978) 667-8700
FAX: (978) 670-9001
e-mail: sales@sipex.com